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1 Software environment for a multiprocessor DSP

Asawaree Kalavade, Joe Othmer, Bryan Ackland, K. J. Singh

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(72.06 KB) Additional Information: full citation, references, citings, index terms

Keywords: RTOS, media processor, multiprocessor DSP, runtime kernel, software environment

2 The network architecture of the Connection Machine CM-5 (extended abstract)

Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, Robert Zak

June 1992 **Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures**

Full text available: pdf(2.00 MB) Additional Information: full citation, references, citings, index terms

3 Fast prototyping: a system design flow applied to a complex system-on-chip multiprocessor design

Benoit Clement, Richard Hersemeule, Etienne Lantreibecq, Bernard Ramanadin, Pierre Coulomb, Francois Pogodalla

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(78.99 KB) Additional Information: full citation, references, citings, index terms

Keywords: fast prototyping, hardware/software (HW/SW) co-design, system design, system modeling, system verification, virtual component (VC) re-use

4 The Starfire SMP interconnect

Alan Charlesworth, Nicholas Aneshansley, Mark Haakmeester, Dan Drogichen, Gary Gilbert, Ricki Williams, Andrew Phelps

November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available: pdf(273.52 KB) Additional Information: full citation, abstract, references, citings

The Starfire interconnect extends the envelope of Unix symmetric multiprocessor (SMP) systems in several dimensions. **Interconnect:** an active centerplane with four address routers and a 16x16 data crossbar provides 64 UltraSPARC processors with uniform memory access at a bandwidth of 10,667 M ps. **Flexibility:** Starfire can be dynamically

reconfigured into multiple hardware-protected operating system domains. **Robustness:** Failing boards can be hot swapped without interrupting sy ...

Keywords: SMP, UMA, bandwidth, domains, interconnect, latency, partitions

5 Multiprocessor SoC MPSoC solutions/nightmare: Flexible architectures for engineering successful SOCs

Chris Rowen, Steve Leibson

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(96.22 KB) Additional Information: full citation, abstract, index terms

This paper focuses on a particular SOC design technology and methodology, here called the advanced or processor-centric SOC design method, which reduces the risk of SOC design and increases ROI by using configurable processors to implement on-chip functions while increasing the SOC's flexibility through software programmability. The essential enabler for this design methodology is automatic processor generation-the rapid and easy creation of new microprocessor architectures, complete with effici ...

Keywords: MPSOC, RISC, RTL, SOC, processor cores

6 An overview of the BlueGene/L Supercomputer

NR Adiga, G Almasi, GS Almasi, Y Aridor, R Barik, D Beece, R Bellofatto, G Bhanot, R Bickford, M Blumrich, AA Bright, J Brunheroto, C Caşcaval, J Castaños, W Chan, L Ceze, P Coteus, S Chatterjee, D Chen, G Chiu, TM Cipolla, P Crumley, KM Desai, A Deutsch, T Domany, MB Dombrowa, W Donath, M Eleftheriou, C Erway, J Esch, B Fitch, J Gagliano, A Gara, R Garg, R Germain, ME Giampapa, B Gopalsamy, J Gunnels, M Gupta, F Gustavson, S Hall, RA Haring, D Heidel, P Heidelberger, LM Herger, D Hoenicke, RD Jackson, T Jamal-Eddine, GV Kopcsay, E Krevat, MP Kurhekar, AP Lanzetta, D Lieber, LK Liu, M Lu, M Mendell, A Misra, Y Moatti, L Mok, JE Moreira, BJ Nathanson, M Newton, M Ohmacht, A Oliner, V Pandit, RB Pudota, R Rand, R Regan, B Rubin, A Ruehli, S Rus, RK Sahoo, A Sanomiya, E Schenfeld, M Sharma, E Shmueli, S Singh, P Song, V Srinivasan, BD Steinmacher-Burow, K Strauss, C Surovic, R Swetz, T Takken, RB Tremaine, M Tsao, AR Umamaheshwaran, P Verma, P Vranas, TJC Ward, M Wazlowski, W Barrett, C Engel, B Drehmel, B Hilgart, D Hill, F Kasemkhani, D Krolak, CT Li, T Liebsch, J Marcella, A Muff, A Okomo, M Rouse, A Schram, M Tubbs, G Ulsh, C Wait, J Wittrup, M Bae, K Dockser, L Kissel, MK Seager, JS Vetter, K Yates

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(357.61 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper gives an overview of the BlueGene/L Supercomputer. This is a jointly funded research partnership between IBM and the Lawrence Livermore National Laboratory as part of the United States Department of Energy ASCI Advanced Architecture Research Program. Application performance and scaling studies have recently been initiated with partners at a number of academic and government institutions, including the San Diego Supercomputer Center and the California Institute of Technology. This mass ...

7 Retrospective: the MIT Alewife machine: architecture and performance

Anant Agarwal

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(1.02 MB) Additional Information: full citation, references, index terms

8 Fast prototyping: a system design flow for fast design, prototyping and efficient IP reuse

Francois Pogodalla, Richard Hersemeule, Pierre Coulomb

March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**

Full text available: pdf(442.98 KB) Additional Information: full citation, references, citings, index terms

Keywords: HW/SW co-design, HW/SW co-verification, RTC, emulation, system modeling, virtual components

9 Experience Using Multiprocessor Systems—A Status Report
Anita K. Jones, Peter Schwarz
June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2

Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

10 Static scheduling algorithms for allocating directed task graphs to multiprocessors
Yu-Kwong Kwok, Ishfaq Ahmad
December 1999 **ACM Computing Surveys (CSUR)**, Volume 31 Issue 4

Full text available: pdf(723.58 KB) Additional Information: full citation, abstract, references, citings, index terms

Static scheduling of a program represented by a directed task graph on a multiprocessor system to minimize the program completion time is a well-known problem in parallel processing. Since finding an optimal schedule is an NP-complete problem in general, researchers have resorted to devising efficient heuristics. A plethora of heuristics have been proposed based on a wide spectrum of techniques, including branch-and-bound, integer-programming, searching, graph-theory, randomization, genetic ...

Keywords: DAG, automatic parallelization, multiprocessors, parallel processing, software tools, static scheduling, task graphs

11 Multiprocessor software design
Peter Hibbard
January 1980 **Proceedings of the ACM 1980 annual conference**

Full text available: pdf(669.64 KB) Additional Information: full citation, abstract, references, index terms

Machines intended for parallel computations exhibit a wide variety of architectural designs, including pipeline, vector and array organizations, less traditional associative, data-flow and systolic organizations, and shared-memory MIMD organizations. It is not surprising, therefore, that the software support for these machines exhibits a wide variety of features reflecting the differing designs. Even within a single class of parallel machine, the system software used on different machines w ...

12 Multiprocessor Organization—a Survey
Philip Enslow
January 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1

Full text available: pdf(1.79 MB) Additional Information: full citation, references, citings, index terms

13 Disco: running commodity operating systems on scalable multiprocessors
Edouard Bugnion, Scott Devine, Kinshuk Govil, Mendel Rosenblum
November 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 4

Full text available: pdf(400.76 KB) Additional Information: full citation, abstract, references, citings, index terms, review

In this article we examine the problem of extending modern operating systems to run efficiently on large-scale shared-memory multiprocessors without a large implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine monitors. We use virtual machines to run multiple commodity operating systems on a scalable multiprocessor. This solution addresses many of the challenges facing the system software for these machines. We demonstrate our approach with a prototy ...

Keywords: scalable multiprocessors, virtual machines

14 Tolerating latency in multiprocessors through compiler-inserted prefetching

Todd C. Mowry

February 1998 **ACM Transactions on Computer Systems (TOCS)**, Volume 16 Issue 1

Full text available: pdf(410.70 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The large latency of memory accesses in large-scale shared-memory multiprocessors is a key obstacle to achieving high processor utilization. Software-controlled prefetching is a technique for tolerating memory latency by explicitly executing instructions to move data close to the processor before the data are actually needed. To minimize the burden on the programmer, compiler support is needed to automatically insert prefetch instructions into the code. A key challenge when ...

Keywords: compiler optimization, prefetching

15 Effective cache prefetching on bus-based multiprocessors

Dean M. Tullsen, Susan J. Eggers

February 1995 **ACM Transactions on Computer Systems (TOCS)**, Volume 13 Issue 1

Full text available: pdf(2.30 MB) Additional Information: full citation, abstract, references, citings, index terms

Compiler-directed cache prefetching has the potential to hide much of the high memory latency seen by current and future high-performance processors. However, prefetching is not without costs, particularly on a shared-memory multiprocessor. Prefetching can negatively affect bus utilization, overall cache miss rates, memory latencies and data sharing. We simulate the effects of a compiler-directed prefetching algorithm, running on a range of bus-based multiprocessors. We show that, despite a ...

Keywords: bus-based multiprocessors, cache prefetching, false sharing, memory latency hiding

16 Cache coherence in large-scale shared-memory multiprocessors: issues and comparisons

David J. Lilja

September 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 3

Full text available: pdf(3.12 MB) Additional Information: full citation, references, citings, index terms

17 Algorithms for scalable synchronization on shared-memory multiprocessors

John M. Mellor-Crummey, Michael L. Scott

February 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 1

Full text available: pdf(3.07 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Busy-wait techniques are heavily used for mutual exclusion and barrier synchronization in shared-memory parallel programs. Unfortunately, typical implementations of busy-waiting tend to produce large amounts of memory and interconnect contention, introducing performance bottlenecks that become markedly more pronounced as applications scale. We argue that this problem is not fundamental, and that one can in fact construct busy-wait synchronization algorithms that induce no memory or interc ...

18 Architectural primitives for a scalable shared memory multiprocessor

Joonwon Lee, Umakishore Ramachandran

June 1991 **Proceedings of the third annual ACM symposium on Parallel algorithms and architectures**

Full text available: pdf(1.27 MB) Additional Information: full citation, references, citings, index terms

19 Waiting algorithms for synchronization in large-scale multiprocessors

Beng-Hong Lim, Anant A[illegible]rwal

August 1993 **ACM Transactions on Computer Systems (TOCS)**, Volume 11 Issue 3

Full text available: pdf(2.72 MB) Additional Information: full citation, abstract, references, citings, index terms

Through analysis and experiments, this paper investigates two-phase waiting algorithms to minimize the cost of waiting for synchronization in large-scale multiprocessors. In a two-phase algorithm, a thread first waits by polling a synchronization variable. If the cost of polling reaches a limit Lpoll and further waiting is necessary, the thread is blocked, incurring an additional fixed cost, B. The choice of Lpoll

Keywords: barriers, blocking, competitive analysis, locks, producer-consumer synchronization, spinning, waiting time

20 Multiprocessor hardware: An architectural overview

John Tartar

January 1980 **Proceedings of the ACM 1980 annual conference**

Full text available: pdf(797.11 KB) Additional Information: full citation, abstract, references, index terms

The subject of multiprocessor computer systems has been discussed almost since the inception of the modern digital computer in its uniprocessor form. The motivation for multiprocessor system research and development activity arises from a consideration of one or more of the following factors: throughput flexibility extendability price/performance availability reliability fault tolerance. While any one of ...

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1 **A general method for deflection worm routing on meshes based on packet routing algorithms**
Roberts, A.; Symvonis, A.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 8 , Issue: 8 , Aug. 1997
Pages:781 - 789

[Abstract] [PDF Full-Text (172 KB)] **IEEE JNL**

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2 **On bit-serial packet routing for the mesh and the torus**
Makedon, F.; Simvonis, A.;
Frontiers of Massively Parallel Computation, 1990. Proceedings., 3rd Symposium on the , 8-10 Oct. 1990
Pages:294 - 302

[Abstract] [PDF Full-Text (688 KB)] **IEEE CNF**

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1 **A three-million-transistor microprocessor**
Abu-Nofal, F.; Avra, R.; Bhabuthmal, K.; Bhamidipaty, R.; Blanck, G.; Charnas, A.; DelVecchio, P.; Grass, J.; Grinberg, J.; Hayes, N.; Haber, G.; Hunt, J.; Kizhepat, G.; Malamy, A.; Marston, A.; Mehta, K.; Nanda, S.; Van Nguyen, H.; Patel, R.; Ray, A.; Reaves, J.; Rogers, A.; Rusu, S.; Shay, T.; Sidharta, I.; Tham, T.; Tong, P.; Trauben, R.; Wong, A.; Yee, D.; Maan, N.; Steiss, D.; Youngs, L.;
Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC, 1992 IEEE International , 19-21 Feb. 1992
Pages:108 - 109, 257

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

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2 **Blue Gene/L, a system-on-a-chip**
Almasi, G.; Almasi, G.S.; Beece, D.; Bellofatto, R.; Bhanot, G.; Bickford, R.; Blumrich, M.; Bright, A.A.; Brunheroto, J.; Cascaval, C.; Castanos, J.; Ceze, L.; Coteus, R.; Chatterjee, S.; Chen, D.; Chiu, G.; Cipolla, T.M.; Crumley, P.; Deutsch, A.; Dombrowa, M.B.; Donath, W.; Eleftheriou, M.; Fitch, B.; Gagliano, J.; Gara, A.; Germain, R.; Giampapa, M.E.; Gupta, M.; Gustavson, F.; Hall, S.; Haring, R.A.; Heidel, D.; Heidelberger, P.; Herger, L.M.; Hoenicke, D.; Jamal-Eddine, T.; Kopcsay, G.V.; Lanzetta, A.P.; Lieber, D.; Lu, M.; Mendell, M.; Mok, L.; Moreira, J.; Nathanson, B.J.; Newton, M.; Ohmacht, M.; Rand, R.; Regan, R.; Sahoo, R.; Sanomiya, A.; Schenfeld, E.; Singh, S.; Song, P.; Steinmacher-Burow, B.D.; Strauss, K.; Swetz, R.; Takken, T.; Tremaine, R.B.; Tsao, M.; Vranas, P.; Ward, T.J.C.; Wazlowski, M.; Brown, J.; Liebsch, T.; Schram, A.; Ulsh, G.;
Cluster Computing, 2002. Proceedings. 2002 IEEE International Conference on , 23-26 Sept. 2002
Pages:349 - 350

[Abstract] [PDF Full-Text (175 KB)] **IEEE CNF**

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1 **The iconic interface for the PIctorial C language**
Di Gesu, V.; Tegolo, D.;
Visual Languages, 1992. Proceedings., 1992 IEEE Workshop on , 15-18 Sept. 1992
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[Abstract] [PDF Full-Text (480 KB)] **IEEE CNF**

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2 **The design of DARTS: a dynamic debugger for multiprocessor real-time applications**
Timmerman, M.; Gielen, F.J.A.;
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[Abstract] [PDF Full-Text (556 KB)] **IEEE JNL**

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3 **Rapid prototyping for DSP systems with multiprocessors**
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Design & Test of Computers, IEEE , Volume: 8 , Issue: 2 , June 1991
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[Abstract] [PDF Full-Text (944 KB)] **IEEE JNL**

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4 **The ParaScope parallel programming environment**
Cooper, K.D.; Hall, M.W.; Hood, R.T.; Kennedy, K.; McKinley, K.S.; Mellor-Crummey, J.M.; Torczon, L.; Warren, S.K.;
Proceedings of the IEEE , Volume: 81 , Issue: 2 , Feb. 1993
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[Abstract] [PDF Full-Text (1984 KB)] **IEEE JNL**

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5 **Detecting nondeterminacy in parallel programs**
Emrath, P.A.; Ghosh, S.; Padua, D.A.;
Software, IEEE , Volume: 9 , Issue: 1 , Jan. 1992
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[Abstract] [PDF Full-Text (1376 KB)] **IEEE JNL**

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6 **Integrating different tools to develop multiprocessor real-time systems**
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7 **A generic tool-set for SoC multiprocessor debugging and synchronization**
Wieferink, A.; Kogel, T.; Leupers, R.; Meyr, H.; Nohl, A.; Hoffman, A.;
Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE International Conference on , 24-26 June 2003
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8 **Dynamic interface for machine vision systems**
Tegolo, D.; Lenzitti, B.; Isgro, F.; Di Gesu, V.;
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[Abstract] [PDF Full-Text (400 KB)] IEEE CNF

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9 **Testing software through real-time model of the plant an experimental example**
Matuonto, M.; Monti, A.; Torri, G.;
Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on , Volume: 3 , 5-9 Sept. 1994
Pages:1807 - 1812 vol.3

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10 **Software abort and multiprocessor debugging**
Baek Youngsik; Jin Sungil;
TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering.1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993
Pages:237 - 241 vol.1

[Abstract] [PDF Full-Text (300 KB)] IEEE CNF

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11 **The design of DARTS: a dynamic debugger for multiprocessor real-time applications**
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Real Time Systems, 1991. Proceedings., Euromicro '91 Workshop on , 12-14 June 1991
Pages:153 - 161

[Abstract] [PDF Full-Text (520 KB)] IEEE CNF
